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KED & ASSOCIATES, LLP
P.O. Box 221200
Chantilly, VA 20153-1200

EXAMINER	
SITTA, GRANT	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,417	CHO ET AL.	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/05/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8 and 10-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8 and 10-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear whether Applicant intended claim 37 to depend from claim 1 or to be independent. Applicant has repeated claim limitations (i.e. panel, voltage source). For purpose of examination, examiner is going to assume claim 37 depends from claim 1 however; examiner is going to assume applicant did not intend duplicate elements.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,4-8, 10-17, 19-30, 32-35, and 37-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Mccormack et al (2002/0041275) hereinafter, Mccormack.

4. In regards to claim 1, Mccormack teaches a plasma display, comprising:

a panel [0003];

at least one voltage source for supplying a sustain voltage to the panel (fig. 1 Vcc);

an inductor for recovering an energy stored in the panel by a resonance phenomenon such that the recovered energy is reusable for driving the panel (fig. 1 L1 and [0037]; and

first and second switches arranged, in parallel (fig.1 S4 and S1 respectfully), between the inductor and the panel (fig. 1 L1 and PS), wherein the inductor stores energy recovered from the panel when the first switch is on and the inductor applies the stored energy to the panel when the second switch is on, and wherein the inductor stores the energy, at a time when a sustain voltage supplied to the panel is clamped at a predetermined voltage ([0037] "[e]nergy is then sent to the load CL from the buffer CB via the inductor L1 in a resonant way. When the switch S1 closes, the floating end of the inductor (the node Nj) is clamped to the buffer voltage Vb via the diode D1. Current then builds up through the inductor L1 until the load voltage Vc equals the buffer voltage Vb at the instant t2.")

5. In regards to claim 5, Mccormack teaches an energy recovering method for a plasma display, comprising [abstract]:

forming a first electrically conductive path between a first voltage source and the plasma display using a first switch (fig. 1 S1 [0037] t1);

forming a second electrically conductive path between a second voltage source and the plasma display using a second switch (fig. 1 S4 [0037] t4);

forming a third electrically conductive path between the inductor and the plasma display using a third switch (fig. 1 S2 [0037]) ; and

forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected, in parallel, to the third switch (fig. 1 S5 [0037]), said method further comprising:

shutting off a backward current from the plasma display using a first diode connected between the third switch and the plasma display (fig. 1 D1); and

shutting off a backward current from the fourth switch using a second diode connected between the fourth switch and the plasma display (fig. 1 D6 [0037]).

6. In regards to claim 7, Mccormack teaches a plasma display comprising:

a display having a plurality of electrodes and having a corresponding display capacitance between first and second nodes [0024];

an inductor coupled to the second node and a third node (fig. 1 L);

a first switch coupled between the first and third nodes (fig. 1 S1 [0037]); and

a second switch (fig. 1 S4 [0037]) coupled between the first and third nodes, the first and second switches being formed in parallel ([0024]), wherein a first current path is formed via the panel capacitance (fig. 1 Cl [0035]), the second node, the inductor, the third node, the first switch and the first node, and a second current path is formed via the panel capacitance, the first node, the second switch, the third node, the inductor and the second node [0024 and 0037], and

wherein the second current path passes energy from the panel capacitance for storage in the inductor when the second switch is on, and the first current path applies the stored energy from the inductor to the panel capacitance when the first switch is on [0024 and 0038].

7. In regards to claim 19, Mccormack teaches a display panels having panel electrodes and corresponding panel capacitance between first and second nodes, an inductor (fig. 1 L1) coupled to the second node and a third node, a first switch (fig. 1 S1) coupled between the first and third nodes and a second switch (fig. 1 S4) coupled between the first and third nodes, the first and second switches being formed in parallel ([0024]), an energy efficient method of driving said display panels through the inductor coupled to the panel electrodes [abstract], comprising:

(a) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a first current path formed via the panel capacitance [0037], the second node, the inductor, the third node, the first switch and the first node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero via the first current path [0037]; and

(b) discharging the panel capacitance through said inductor initially while storing energy in said inductor until the magnitude of the inductor current reaches a maximum through a second current path formed via the panel capacitance, the first node, the

second switch, the third node, the inductor and the second node, and secondly charging the panel capacitance through said inductor while removing the stored energy from said inductor until the inductor current reaches zero or before zero through the second current path [0037],

wherein said inductor stores said energy while the panel capacitance is clamped at first predetermined voltage and wherein said energy is removed from said inductor to cause the panel capacitance to change to a second predetermined voltage [0037].

8. In regards to claim 25, Mccormack teaches a plasma display panel driver circuit comprising:

a panel inter-electrode capacitor (fig. 1 CL) provided between at least one of a plurality of scanning electrodes and a plurality of sustain electrodes of a panel [0035];

a charging/discharging circuit connected in series with said panel inter-electrode capacitor and between first and second nodes (fig. 1 S1 and S4),

a clamping circuit having first and second (fig. 1 S2 and S5) switches for clamping a terminal voltage across the panel inter-electrode capacitor to a first power source voltage level (Vcc) and to a second power source voltage level (Vb i.e. Vcc/2), said first switch being connected in series between the first node and the first power source voltage level (fig. 1 S2), said second switch being connected in series between said first node and the second power source voltage level (fig. 1 S5), said inter-electrode capacitor being connected in series to the first and second nodes and said

charging/discharging circuit and said clamping circuit being coupled in parallel between the first and second nodes (fig. 1 CL),

wherein said charging/discharging circuit comprises a pair of switches coupled in parallel (fig. 1 S2 and S5) to each other between the first anode and a third node and an inductive coil coupled in series between the second and third nodes (fig. 1 L1), and wherein the inductive coil stores energy recovered from the panel inter-electrode capacitor when a first one of the pair of switches is turned on and the inductive coil applies the stored energy to the panel inter-electrode capacitor when a second one of the pair of switches is turned on [0037].

9. In regards to claim 34, Mccormack teaches a plasma display comprising:

a panel [003, 0035];

at least one voltage source for supplying a sustain voltage to the panel (fig. 1 Vcc):

an inductor for recovering an energy (fig. 1 L1), stored in the panel by a resonancephenomenon such that the recovered energy, is reusable for driving the panel [0037]; and

first and second switches arranged, in parallel, between the inductor and the panel wherein the inductor stores energy, recovered from the panel when the first switch is on and the inductor applies the stored energy, to the panel when the second switch is on (fig. 1 S1 and S4) wherein the panel includes a panel capacitor and wherein

the inductor is the only circuit element for storing energy recovered from the panel capacitor [0037].

10. In regards to claim 39, Mccormack teaches an energy recovery method or a plasma display (abstract), comprising:

forming a first electrically conductive path between a first voltage source and the plasma display using a first switch (fig. 1 S1 [0024 and 0037]);

forming a second electrically conductive path between a second voltage source and the plasma display using a second switch (fig. 1 S4 [0024 and 0037]);;

forming a third electrically conductive path between the inductor and the plasma display using a third switch (fig. 1 S5 [0037]); and

forming a fourth electrically conductive path between the inductor and the plasma display using a fourth switch connected, in parallel, to the third switch (fig. 1 S2),

wherein the third switch has a first terminal coupled to the inductor and a second terminal coupled to the plasma display, and wherein the fourth switch has one terminal coupled to the first terminal of the third switch and another terminal coupled to the second terminal of the third switch [0037]. Examiner notes the claim language does not require the elements to be directly coupled.

11. In regards to claim 4, Mccormack teaches further comprising:
a first diode connected between the first switch and the panel; and a second diode connected between the second switch and the panel (fig. 1 D1 and D6).

12. In regards to claim 8, Mccormack teaches wherein the direction of the first and second current paths are opposite directions [0024].

13. In regards to claim 10, Mccormack teaches wherein the display capacitance is charge or discharged based on an LC resonance frequency [0024].

14. In regards to claim 11, Mccormack teaches wherein the display capacitance is charged or discharged based on a non-LC resonance frequency [0037]. Examiner note the non-LC frequency in which the capacitance is charged or discharged is based on the switches.

15. In regards to claim 12 Mccormack teaches wherein an energy of the inductor current is increased prior to the discharging of the display capacitance or *the energy is decreased prior to charging of the display capacitance* [0037]. Examiner notes the remaining energy in the inductor is supplied to the load capacitor and thus decreased.

16. In regards to claim 13, Mccormack teaches wherein during charging or discharging, the display capacitance is clamped before a stored energy of inductor

reaches zero [0036].

17. In regards to claim 14, Mccormack teaches wherein the first current path further comprises a diode coupled between the first switch and the first node (fig. 1 D1).

18. In regards to claim 15, Mccormack teaches wherein the second current path further comprises a diode coupled between the first node and the second switch (fig. 1 D2).

19. In regards to claim 16, Mccormack teaches further comprising: a first clamping circuit coupled between the first and second nodes (fig. 1 S2, D2 and R2); and a second clamping circuit coupled between the first and second nodes (fig. 1 S5, D8 and R5).

20. In regards to claim 17, Mccormack teaches wherein the first clamping circuit comprises a third switch coupled to the first node and a first potential via a first conductive path (fig. 1 S2, D2 and R2), and the second clamping circuit comprises a fourth switch coupled to the first node and a second potential via a second conductive path, wherein the first and second potentials are different (fig. 1 S5, D8 and R5).

21. In regards to claim 20, Mccormack teaches further comprising: maintaining panel capacitance after step (a) by a first clamping circuit having a third switch coupled to the first node and a first potential via a first conductive path (fig.

1 S2, D2 and R2); and maintaining the panel capacitance after step (b) by a second clamping circuit having a fourth switch coupled to the first node and a second potential via a second conductive path (fig. 1 S5, D8 and R5).

22. In regard to claim 21, Mccormack teaches wherein storing and removing of stored energy in the inductor is based on an LC resonance frequency if the inductor current reaches zero [0024].

23. In regards to claim 22, Mccormack teaches wherein charging and discharging of the panel capacitance is not based on an LC resonance frequency via the first and second clamping circuit clamping the panel capacitance prior to the inductor current reaching zero [0037]. Examiner note the non-LC frequency in which the capacitance is charged or discharged is based on the switches and t4.

24. In regards to claim 23, Mccormack teaches wherein the first and second clamping circuits clamp the panel capacitance prior to the inductor current reaches zero [0037]. S2 closes just before the end of the recovery cycle.

25. In regards to claim 24, Mccormack teaches wherein the second clamping circuit pre-stores energy in the inductor prior to step (a) and the first clamping circuit pre-stores energy in the inductor prior to step (b) [0038].

26. In regards to claim 26, Mccormack teaches wherein each of the pair of switches comprises a first transistor and a diode, and the pair of switches provide opposite current paths (fig. 1 S1 and S4; D6 and D1).

27. In regards to claim 27, Mccormack teaches wherein the inter- electrode capacitor is charged/discharged based on an LC resonant frequency of the inductor coil and the inter-electrode capacitor [0024].

28. In regards to claim 28, Mccormack teaches wherein the inter- electrode capacitor is charge/discharged based on a non-LC resonant frequency of the inductor coil and the inter-electrode capacitor [0037]. Examiner note the non-LC frequency in which the capacitance is charged or discharged is based on the switches and t4.

29. In regards to claim 29, Mccormack teaches wherein the clamping circuit clamps the inter-electrode capacitor one of the first and second power source voltage level prior to an energy of the inductor coil reaching zero [0037]. S2 closes just before the end of the recovery cycle.

30. In regards to claim 30, Mccormack teaches wherein the clamping circuit increases an energy of the inductor coil prior to charging/discharging of the inter-electrode capacitor [0037].

31. In regards to claim 32, Mccormack teaches wherein the inductor stores the energy during a time when the sustain voltage supplied to the panel is clamped at a negative voltage [0037]. Examiner notes the second to last paragraph of 0037 wherein the negative current through the inductor.

32. In regards to claim 33, Mccormack teaches wherein the second switch is turned on to allow the inductor to apply the stored energy to the panel when the sustain voltage is to rise to a positive voltage (fig. 1 S2 [0037]).

33. In regards to claim 35, Mccormack teaches wherein the inductor is to store energy recovered from the panel capacitor at a time when a sustain voltage supplied to the panel is clamped at a negative voltage [0037], and wherein the inductor is to apply the stored energy to the panel capacitor during at a time when the sustain voltage is to rise to a positive polarity (fig. 2 IL [0037-0038]).

34. In regards to claim 37, Mccormack teaches a plasma display as claimed in claim 1, wherein the first switch has a first terminal (fig. 1 S4) coupled to the inductor (fig. 1 (L1)) and a second terminal coupled to the panel(fig. 1 CL) , and wherein the second switch (fig. 1 S1) has one terminal coupled to the first terminal of the first switch and another terminal coupled to the second terminal of the first switch(fig. 1 S4). Examiner notes the terminals are coupled together and Applicant is not claiming wherein the terminals are directly or immediately coupled together.

35. In regards to claim 38, Mccormack teaches wherein the second terminal of the first switch is coupled to the panel through a first diode (fig. 1 S4 and D6), and wherein said another terminal of the second switch is coupled to the panel through a second diode (fig. 1 S1 and D1).

36. In regards to claim 40, Mccormack teaches wherein the second terminal of the third switch is coupled to the plasma display through a first diode (fig. 1 S2 [0037] and D2), and wherein said another terminal of the fourth switch is coupled to the panel through a second diode (fig. 1 S5 [0037] and D8).

Claim Rejections - 35 USC § 103

37. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mccormack, in view of Lee et. al (US 20030025459) hereinafter, Lee.

39. In regards to claim 36, Mccormack teaches a plasma display comprising:

a panel [003, 0035];

at least one voltage source for supplying a sustain voltage to the panel (fig. 1 Vcc):

an inductor for recovering an energy (fig. 1 L1), stored in the panel by a resonance phenomenon such that the recovered energy, is reusable for driving the panel [0037]; and

first and second switches arranged, in parallel, between the inductor and the panel, wherein the inductor stores energy, recovered from the panel when the first switch is on and the inductor applies the stored energy, to the panel when the second switch is on (fig. 1 S1 and S4),

wherein at least one voltage source comprises: a first voltage source for charging the panel to a first polarity, voltage; and a second voltage source for charging the panel to a second polarity voltage (fig. 1 Vcc and Vb)

Mccormack differs from the claimed invention in that Lee does not disclose wherein the first polarity voltage and the second polarity voltage have a same absolute value and are different.

However, Lee teaches a system and method for wherein the first polarity voltage and the second polarity voltage have a same absolute value and are different (fig. 2 Vs and -Vs).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Mccormack to include the use of wherein the first polarity voltage and the second polarity voltage having a same absolute value as taught by Lee in order to prevent the voltage at each end of the inductor from being greater than the power supply and so that the rising time of the panel voltage is equal to the falling time.

40. In regards to claim 2, Mccormack differs from the claimed invention in that Lee does not wherein at least one voltage source comprises: a first voltage source for charging the panel to a first polarity voltage; and a second voltage source for charging the panel to a second polarity voltage different from the first polarity voltage.

However, Lee teaches a system and method for wherein at least one voltage source comprises: a first voltage source for charging the panel to a first polarity voltage; and a second voltage source for charging the panel to a second polarity voltage different from the first polarity voltage. (fig. 2 Vs and -Vs).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Mccormack to include the use of wherein at least one voltage source comprises: a first voltage source for charging the panel to a first polarity voltage; and a second voltage source for charging the panel to a second polarity voltage

different from the first polarity voltage. as taught by Lee in order to prevent the voltage at each end of the inductor from being greater than the power supply and so that the rising time of the panel voltage is equal to the falling time.

41. In regards to claim 3, Mccormack as modified by Lee teaches a third switch (fig. 1 S2 [0037] Mccormack) for forming a conductive path between the first voltage source and the panel (fig. 1 Vcc Mccormack); and a fourth switch (fig. 1 S5 [0037] Mccormack) for forming a conductive path between the second voltage source and the panel (fig. 2 Vs and –Vs Lee).

42. In regards to claim 18, Mccormack differs from the claimed invention in that Lee does not disclose wherein the first potential is provided by a positive power source, and the second potential is provided by a negative power source.

However, Lee teaches a system and method for wherein the first potential is provided by a positive power source, and the second potential is provided by a negative power source. (fig. 2 Vs and -Vs).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Mccormack to include the use of wherein the first potential is provided by a positive power source, and the second potential is provided by a negative power source. as taught by Lee in order to prevent the voltage at each end of the

inductor from being greater than the power supply and so that the rising time of the panel voltage is equal to the falling time.

43. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mccormack, in view of Nagai et. al (US 6,011,355) hereinafter, Nagai.

44. In regards to claim 31, Mccormack differs from the claimed invention in that Mccormack does not disclose wherein each of said first and second switches comprises a transistor.

However, Nagai teaches a system and method for wherein each of said first and second switches comprises a transistor (col. 12, lines 59-60 of Nagai).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Nagai to include the use of wherein each of said first and second switches comprises a transistor as taught by Nagai since transistors as switches offer lower cost and substantial reliability over conventional mechanical relays.

Response to Arguments

45. Applicant's arguments with respect to claims 1-5, 7-8, 10-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Grant D Sitta/
Examiner, Art Unit 2629
January 30, 2009